CMOSTEK

CMT2168A

27 - 960 MHz OOK/(G)FSK Transmitter SoC

MCU Features

- High-performance 8051
  - Single instruction cycle (1T-8051)
  - Up to 24 MIPS
  - 8 kB RAM / 8 kB OTP
  - Built-in 512 bits EEPROM
  - 12 kB ROM (API function library)
  - Single-wire online simulation debugging interface
- Digital peripherals
  - Built-in AES-128 acceleration engine
  - True random number generator
  - 1x UART
  - 1x SPI
  - 1x WDT
  - 1x RTC (internal 32 kHz and external 32.768KHz)
  - 2x 16-bit multifunction timer (supports PWM/CCP)
  - 16x GPIO, all supporting interrupt-on-change and wake-up
- Analog peripherals
  - Sub-1G transmitter module
  - 3D low-frequency wake-up module
  - 12-bit SAR-ADC, 100ksps, 12-ch
  - 2x micro-power operational amplifier (LPOA)
  - 2x high-speed low-power operational amplifier (HSOA)
  - Built-in high speed 3 /12/ 24 MHz RC oscillator
  - Built-in low-power 32 kHz RC oscillator
  - Support for external 32.768 kHz crystal oscillator
- Code security
  - Built-in multi-level program protection achieving high security
  - Serial port (S3S interface) for programming with lock function

Low-power Features

- Operating temperature: - 40 ^{o}C ~ + 85 ^{o}C
- Operating voltage: 2.0 - 3.6 V
- Shutdown current: 300 nA
- RTC mode current: 800 nA
- Low-power wake-up: 4.6 uA @ 125 kHz

Sub-1G Transmitter Features

- Operating frequency range: 27 - 960 MHz
- Modulation mode: OOK, G/FSK
- Data rate
  - 0.5 – 40 kbps (OOK)
  - 0.5 – 200 kbps (G/FSK)
- Output power: +13 dBm (Max.)
- Operating current: 18mA @+13 dBm, 433.92 MHz FSK
- Single-ended and high-efficient Class E high-frequency transmission PA
- PA ramping slope varying according to rate

3D Low-frequency Wake-up Features

- Operating frequency: 20 - 200 kHz
- Data rate: 1 – 8 kbps
- Supporting 1/2/3 channels
- Supporting programmable 8/16/24/32-bit matching sync word
- Supporting programmable 8/16-bit matching ID
- Wake-up sensitivity of 70 uVrms
- Supporting low-power listening mode (DutyCycle)
- Supporting digital RSSI with a dynamic range of 80 dB

Packaging

- QFN32

Application

- Garage door remote control
- Remote access control system
- Consumer wireless remote control
- Smart home
- Home security
- Active RFID tags
- Wireless sensor network
- WM-Bus T1 mode

Description

Embedded with a 1T-8051 core, the CMT2168A is a low-power SoC RF transmitter enriched with below features.

1. The chip series supports wireless transmission @ 27 - 960 MHz with OOK or (G)FSK modulation.
2. High-efficient single-ended PA with an adjustable output power range of 0~+13dBm, consuming only a current of 18 mA for +13dBm transmission.
3. 8 kB OTP program bank and 12 kB ROM (for API library storage).
4. With 1-wire online simulation function, users can download the target debugging code directly to the on-chip PRAM through the dedicated 1-wire debugger, achieving more convenient debugging comparing with the troublesome debugging of traditional OTP chip with no online simulation supporting and a specific simulator required.
5. Supporting built-in AES-128 accelerator, true random number generator (TRNG), and 32-bit serial number (ID), fit for remote or active RFID applications requiring encrypted transmission.
6. Supporting dual-clock operating architecture, namely, the system operating with the internal high-speed clock meanwhile the internal low-power RC oscillation or external 32.768 kHz crystal oscillator operating for periodical wake-up from low-power mode.
7. Built-in 12-bit high-precision and high-speed SAR-ADC, fit for wireless sensor acquisition scenarios.

QFN32 5 x 5 x 0.75 mm

Ordering Information

Model	Package	MOQ
CMT2168A-EQR	QFN32 T&R	3,000 pcs

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1 Electrical Specifications

If nothing else stated, all measurement results are obtained using the evaluation board CMT216xA-EM Rev001 under the conditions of VDD= 3.3 V，T_{OP}= 25°C，F_{RF} = 433.92 MHz, matching to 50 Ω impedance and +10 dBm output power.

1.1 Recommended Operating Conditions

Table 1. Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	VDD	Temperature range is -40℃ ~ +85℃	2.0		3.6	V
Operating temperature	T_{OP}		- 40		+ 85	℃
Supply voltage slope			1			mV/us

1.2 Absolute Maximum Ratings

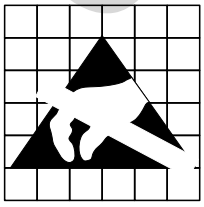
Table 2. Absolute Maximum Ratings [1]

Parameter	Symbol	Condition	Min.	Typ.	Max.
Supply voltage	VDD		-0.3	3.6	V
Interface voltage	VIN		-0.3	VDD + 0.3	V
Junction temperature	TJ		-40	125	℃
Storage temperature	TSTG		-50	150	℃
Soldering temperature	TSDR	Lasts for at least 30 seconds		255	℃
ESD rating[2]		Human body model (HBM)	-2	2	kV
Latch-up current		@ 85℃	-100	100	mA

Notes:

[1]. Exceeding *the Absolute Maximum Ratings* may cause permanent damage to the equipment. This value is a pressure rating and does not imply that the function of the equipment is affected under this pressure condition, but if it is exposed to absolute maximum ratings for extended periods of time, it may affect equipment reliability.

[2]. The CMT216xA is a high performance RF integrated circuit. The operation and assembly of this chip should only be performed with good ESD protection.



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent performance degradation or loss of functionality.

1.3 Transmitter Specifications

Table 3. Transmitter Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	F_{RF}	HXOSC connecting 26 MHz crystal oscillator	27		480	MHz
			630		960	MHz
Data rate	DR	OOK	0.5		40	kbps
		(G)FSK	0.5		200	kbps
Output power range	P_{OUT}	Single-ended PA mode	0		+13	dBm
FSK frequency deviation range	F_{DEV}	630 ~ 960 MHz	1		300	kHz
		315 ~ 480 MHz	0.5		150	kHz
		210 ~ 320 MHz	0.33		100	kHz
		160 ~ 240 MHz	0.25		75	kHz
		105 ~ 160 MHz	0.17		50	kHz
Output power step	P_{STEP}			1		dB
Transmission startup time [1]	T_{PLL}	API tx_sym_prepare_for_transmission execution time		900		uS
FSK transmission current [2]	$I_{DD-315F}$	0dBm		7.9		mA
		+5dBm		10.0		mA
		+7dBm		11.4		mA
		+10dBm		14.0		mA
		+13dBm		17.0		mA
	$I_{DD-434F}$	0dBm		8.0		mA
		+5dBm		10.3		mA
		+7dBm		11.8		mA
		+10dBm		14.3		mA
		+13dBm		20.6		mA
	$I_{DD-868F}$	0dBm		9.2		mA
		+5dBm		12.2		mA
		+7dBm		13.8		mA
		+10dBm		17.7		mA
		+13dBm		23.5		mA
	$I_{DD-915F}$	0dBm		9.1		mA
		+5dBm		12.3		mA
		+7dBm		13.7		mA
		+10dBm		18.3		mA
		+13dBm		25.0		mA
OOK transmission current [3]	$I_{DD-434O}$	0dBm		6.5		mA
		+5dBm		7.2		mA
		+7dBm		7.8		mA
		+10dBm		8.5		mA
		+13dBm		12.0		mA

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
	$I_{DD-868O}$	0dBm		6.8		mA
		+5dBm		8.0		mA
		+7dBm		8.9		mA
		+10dBm		10.5		mA
		+13dBm		13.7		mA
Phase noise	PN_{434}	100kHz frequency deviation		80		dBc/Hz
		200kHz frequency deviation		83		dBc/Hz
		400kHz frequency deviation		91		dBc/Hz
		600kHz frequency deviation		96		dBc/Hz
		1.2MHz frequency deviation		105		dBc/Hz
	PN_{868}	100kHz frequency deviation		-77		dBc/Hz
		200kHz frequency deviation		-79		dBc/Hz
		400kHz frequency deviation		-87		dBc/Hz
		600kHz frequency deviation		-91		dBc/Hz
		1.2MHz frequency deviation		-100		dBc/Hz
Harmonic output	$H2_{315}$	2^{nd} harmonic @630MHz, +13dBm		< -45		dBm
	$H3_{315}$	3^{nd} harmonic @945MHz, +13dBm		< -45		dBm
	$H2_{434}$	2^{nd} harmonic @867.84MHz, +13dBm		< -45		dBm
	$H3_{434}$	3^{nd} harmonic @1301.76MHz, +13dBm		< -45		dBm
	$H2_{868}$	2^{nd} harmonic @1736MHz，+13dBm		< -36		dBm
	$H3_{868}$	3^{nd} harmonic @2604MHz，+13dBm		< -36		dBm
	$H2_{915}$	2^{nd} harmonic @1830MHz，+13dBm		< -36		dBm
	$H3_{915}$	3^{nd} harmonic @2745MHz，+13dBm		< -36		dBm
OOK adjusted extinction ratio				60		dB
Occupied bandwidth	OBW_{315}	A bandwidth of -20 dBc, RBW = 1kHz，SR = 1.2 kbps		6		kHz
	OBW_{434}	A bandwidth of -20 dBc, RBW = 1kHz，SR = 1.2 kbps		7		kHz

Notes

[1]. This item already includes the crystal startup time.

[2]. It includes the 8051 core current. HFOSC uses the internal 24 MHz high-speed RC as the clock source.

[3]. A high/low duty cycle of 50% for baseband data.

1.4 Oscillator Specifications

Table 4. Oscillator Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Parameter
High-speed oscillating frequency	Crystal frequency [1]	F_{HXOSC}			26		MHz
	Frequency precision [2]				±20		ppm
	Load capacitor	$C_{HX-LOAD}$			15		pF
	Equivalent resistance	R_{HX-ESR}				60	Ω
	Startup time [3]	t_{HXOSC}			400		us
32.768 KHz crystal oscillator	Crystal frequency [1]	F_{LXOSC}			32.768		KHz
	Frequency precision [2]						ppm
	Load capacitor	$C_{LX-LOAD}$			9	12.5	pF
	Equivalent resistance	R_{LX-ESR}			50	90	KΩ
	Startup time [3]	t_{LXOSC}			1		s
Internal high speed RC oscillator	RC oscillating frequency	F_{HF_RC}		3	24	24	MHz
	Frequency precision [4]				1		%
Internal 32 kHz RC oscillator	Oscillator frequency	F_{LP_RC}			32		kHz
	Frequency precision [4]				1		%

Notes:

[1]. An external reference clock can be used to drive the XTAL pin directly through a coupling capacitor. It's required the peak-to-peak level of the external reference clock is between 0.3 and 0.7 V.

[2]. It involves:(1) initial tolerance, (2) crystal loading, (3) aging, and (4) temperature changing. The acceptable crystal frequency tolerance is subject to the bandwidth of the receiver and the RF error between the receiver and its paired transmitter.

[3]. This parameter is crystal dependent to a large degree.

[4]. Frequency precision is the value after calibration, which is related to environmental factors. Users can initiate calibration through calling the calibration API.

1.5 EEPROM Specifications

Table 5. EEPROM Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Re- writing time	t_{EE-WR}	Call eeprom_write_words for [1]		14		ms/unit
		Call eeprom_set_dec_count [2]		42		ms
Number of programming times		Call eeprom_write_words [1]	10,000	100,000		cycles
		Call eeprom_set_dec_count [2]		1,000,000		cycles

Notes:

[1]. The internal EEPROM is re-written by calling API eeprom_write_words for direct re-writing, and the operation address points to a 2-byte storage unit, namely, each unit is 2 bytes.

[2]. The internal EEPROM is re-written by calling API eeprom_set_dec_count for enhanced re-writing. By applying Balanced Gray Code algorithm, it can endure more than 1,000,000 writing operations. It should be noted that the function is fixed to operating 3 units, namely, this field occupies 6 bytes with only the lower 22 bits data valid in the written value and the read value.

1.6 3D Low-frequency Wake-up Performance

Table 6. 3D-LF RX Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Low-frequency range	LF_{Range}	Operating frequency range	15	125	200	kHz
Operating current	$I_{single\_carrier\_RC}$	Power consumption when single channel in operating (using internal RC clock for carrier detection)		4.6		uA
	$I_{scan\_carrier\_RC}$	Power consumption when multiple channels in operating		4.6		uA
	$I_{single\_snr\_RC}$	Power consumption when single channel in operating (SNR detection)		5.7		uA
	$I_{scan\_snr\_RC}$	Power consumption when multiple channels in operating		5.7		uA
	$I_{single\_carrier\_EXT}$	Power consumption when single channel in operating (using an external 32.768 kHz crystal clock for carrier detection)		4.8		uA
	$I_{scan\_carrier\_EXT}$	Power consumption when multiple channels in operating		4.8		uA
	$I_{single\_snr\_EXT}$	Power consumption when single channel in operating		5.9		uA
	$I_{scan\_snr\_EXT}$	Power consumption when multiple channels in operating		5.9		uA

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
	I_{RC_DECODE}	Power consumption when decoding (data output is not connected to load)		5.7		uA
	$I_{150/300\_Fix\_DC\_RC}$	Fixed duty cycle mode, RX_time = 150 ms, Sleep_time = 300 ms		2.8		uA
	$I_{150/600\_Fix\_DC\_RC}$	Fixed duty cycle mode, RX_time = 150 ms, Sleep_time = 600 ms		2.4		uA
	$I_{5/10\_Extend\_RC}$	Auto-extended duty cycle mode, Rx_time = 5 ms, Sleep_time = 10 ms		2.9		uA
	$I_{5/20\_Extend\_RC}$	Auto-extended duty cycle mode, Rx_time = 5 ms, Sleep_time = 20ms		2.5		uA
	$I_{5/40\_Extend\_RC}$	Auto-extended duty cycle mode, Rx_time = 5 ms，Sleep_time = 40 ms		2.2		uA
	$I_{5/80\_Extend\_RC}$	Auto-extended duty cycle mode, Rx_time = 5 ms，Sleep_time = 80 ms		2.0		uA
Sensitivity	$S_{carrier}$ carrier detection	Data rate of 1 kbps		65		uVrms
		Data rate of 2 kbps		65		uVrms
		Data rate of 4 kbps		70		uVrms
		Data rate of 8 kbps		80		uVrms
	S_{snr} SNR detection (SNR is set as 8 dB)	Data rate of 1 kbps		70		uVrms
		Data rate of 2 kbps		70		uVrms
		Data rate of 4 kbps		70		uVrms
		Data rate of 8 kbps		70		uVrms
Startup time [2]	T_{LF_STR}	3D-LF RX startup settling time		1		ms

Notes:

[1]. The startup time means the stabilization time dedicated for starting the 3D-LF module after the software initialization is completed.

1.7 High-speed Low-power Op Amplifier (HSOA) Performance

Table 7. HSOA Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input offset voltage	V_{OS}			±1		mV
Input offset voltage temperature drift	dV_{OS}/dT	-40 ～ +85 ℃		±3		uV/℃
Input offset current	I_{OS}			±2		pA
Input bias current	I_B			±1		pA
Full temperature range input bias current	I_B	-40 ～ +85 ℃			±100	pA
Common mode input impedance	Z_{CM}			10^{13}||4		Ω||pF

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Differential mode input impedance	Z_{DIFF}			10^{13}||2		Ω||pF
Common mode input range	V_{CMR}		VSS-0.2		VDD+0.2	V
Common mode rejection ratio	CMRR		80	120		dB
Power supply rejection ratio	PSRR		70	90		dB
Large signal DC open loop gain	A_{OL}	0.3 V ≤ VOUT ≤ VDD-0.3	90	120		dB
Maximum output voltage swing	V_{SW}		VSS+0.05		VDD-0.05	V
Linear output voltage swing	V_{OVR}		VSS+0.2		VDD-0.2	V
Output short circuit current	I_{SC}	VDD = 2.2 V V_{BAT} = VDD = 3.3 V		±11 ±21		mA
Gain bandwidth product	GBWP			3		MHz
Slew rate	SR			1.2		V/uS
Phase margin	PM		70	80		°
Input voltage noise	E_n	1 Hz - 10 kHz		12		uVpp
Input voltage noise density	e_n	@ 1 kHz		160		nV/√Hz
Quiescent Current	I_Q			81		uA
Leakage current	$I_{LEAKAGE}$	Circuit is not in operating		0.35		nA
Settling time	T_{STAB}	The stabilization time of the analog circuit			5	uS

1.8 Micro-power Operational Amplifier (LPOA) Performance

Table 8. LPOA Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input offset voltage	V_{OS}			±2		mV
Input offset voltage temperature drift	dV_{OS}/dT	-40 ～ +85 ℃		±3		uV/℃
Input offset current	I_{OS}			±2		pA
Input bias current	I_B			±1		pA
Full temperature range input bias current	I_B	-40 ～ +85 ℃			±100	pA
Common mode input impedance	Z_{CM}			10^{13}||4		Ω||pF
Differential mode input impedance	Z_{DIFF}			10^{13}||2		Ω||pF
Common mode input range	V_{CMR}		VSS-0.2		VDD+0.2	V
Common mode rejection ratio	CMRR		75	115		dB
Power supply rejection ratio	PSRR		70	90		dB

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Large signal DC open loop gain	A_{OL}	0.3 V ≤ VOUT ≤ VDD-0.3	85	130		dB
Maximum output voltage swing	V_{SW}		VSS+0.05		VDD-0.05	V
Linear output voltage swing	V_{OVR}		VSS+0.2		VDD-0.2	V
Output short circuit current	I_{SC}	VDD = 2.2 V V_{BAT} = VDD = 3.3 V		±11 ±21		mA
Gain bandwidth product	GBWP			24		kHz
Slew rate	SR			10		V/mS
Phase margin	PM		70	80		°
Input voltage noise	E_n	1 Hz - 1k Hz		14		uVpp
Input voltage noise density	e_n	@ 1 kHz		345		nV/√Hz
Quiescent current	I_Q			0.84		uA
Leakage current	$I_{LEAKAGE}$	Circuit is not in operating		0.32		nA
Settling time	T_{STAB}	The stabilization time of the analog circuit		100	200	uS

1.9 High-precision ADC Performance

Table 9. High-precision ADC Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	R_{ADC}			12		bit
Effective number of bits	NOEB			10		bit
Conversion input range	V_{AIN}		0		V_{REF}	V
ADC clock frequency	f_{ADC}		0.5	1.0	2.0	MHz
ADC total conversion time Sampling time [1] Successive approximation conversion time [2] Data update time	t_{CONV} t_{SAMP} t_{SAR} t_{UPDATE}		16 2 13 1	16 2 13 1	25 8 16 1	$1/F_{ADC}$
ADC data refresh rate	f_S	F_{ADC} = 1 MHz		62.5		kHz
Stabilization time [3]	t_{STAB}				10	uS
Offset error	E_{OS}	F_{ADC} = 1 MHz		±4		LSB
Gain error	E_G	F_{ADC} = 1 MHz		±4		LSB
Integral nonlinearity error	INL	F_{ADC} = 1 MHz		±3		LSB

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Differential nonlinearity error	DNL	F_{ADC} = 1 MHz		±2		LSB
ADC reference voltage Regulator output Bandgap reference External input reference [4]	V_{REF}	 Input from B6 pin	 1.0	 V_{DDA} 1.2	 V_{DDA}	V
Supply voltage range	V_{BAT}		2.0		3.6	V
Operating voltage range	V_{DDA}		2.0	2.2	3.6	V
Operating current	I_{ADC}	V_{DDA} = 2.2 V		220		uA
Power efficiency	P_E			7.6		pJ/Conv
Leakage current	$I_{LEAKAGE}$			2.2		nA

Notes:

[1]. The sampling time can be configured by software. See *AN281 CMT216xA ADC and AFE User Guide* or *CMT216xA User Guide* for details.

[2]. The successive approximation conversion time can be configured by software. See *AN281 CMT216xA ADC and AFE User Guide* or *CMT216xA User Guide* for details.

[3]. The stabilization time refers to the analog circuit stabilization time after power-on, which depends on the system design.

[4]. The external input reference voltage must be at least 1.0 V, otherwise the circuit may not work properly.

1.10 Temperature Sensor Specifications

Table 10. Temperature Sensor Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Temperature measurement error [1]	T_{ERR}	VDD：2.2 ~ 3.6 V TOP：-20 ~ +70 ℃		TBD		℃
		VDD：2.2 ~ 3.6 V TOP：-40 ~ +125 ℃		TBD		
Temperature sensor circuit establishing time	t_{STAB}				5	us

Notes:

[1]. Based on the average of two measurements.

1.11 Supply Voltage Detection Specifications

Table 11. Supply Voltage Detection Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Battery measuring error [1]	V_{ERR}		-50		+50	mV
Battery sensor circuit establishing time	t_{STAB}				5	us

Notes:

[1]. Based on the average of two measurements.

1.12 Constant Current Source Drive Specifications

Table 12. Constant Current Source Drive Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
D2 port constant current driver current[1]	I_{D2_DRV}		0		+250	mA
D2 port current output error range	I_{D2_ERR}	Full output range		+10		%
D3 port constant current driver current[1]	I_{D3_DRV}		0		+40	mA
D3 port current output error range	I_{D3_ERR}	Full output range		+10		%
Constant current source driver establishing time	t_{DRV_STAB}			5		uS

Notes:

[1]. The constant current source output current of D2 and D3 is adjustable. See *AN281 CMT216xA ADC and AFE User Guide* or *CMT216xA User Guide* for details.

1.13 Micro-power Regulator Specifications

Table 13. Micro-power Regulator Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage	V_{REG_OUT}			2.2		V
Output drive current	I_{REG_OUT}				0.5	mA
Quiescent Current	I_{REG_Q}			2.3		uA
Setup time	t_{REG_STAB}				200	uS

1.14 DC Specifications

Table 14. DC Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Active mode operating current [1] (HFOSC = 24 MHz)	I_{AM_24}	CLK_SYS_DIV=1, F_{SYSCLK}=24 MHz		2.15		mA
		CLK_SYS_DIV=2, F_{SYSCLK}=12 MHz		1.56		mA
		CLK_SYS_DIV=4, F_{SYSCLK}=6 MHz		1.25		mA
		CLK_SYS_DIV=8, F_{SYSCLK}=3 MHz		1.09		mA
		CLK_SYS_DIV=16, F_{SYSCLK}=1.5 MHz		1.00		mA
Active mode operating current (HFOSC = 12 MHz)	I_{AM_12}	CLK_SYS_DIV=1, F_{SYSCLK}=12 MHz		1.22		mA
		CLK_SYS_DIV=2, F_{SYSCLK}=6 MHz		0.91		mA
		CLK_SYS_DIV=4, F_{SYSCLK}=3 MHz		0.75		mA
		CLK_SYS_DIV=8, F_{SYSCLK}=1.5 MHz		0.67		mA
Active mode operating current (HFOSC = 3 MHz)	I_{AM_3}	CLK_SYS_DIV=1, F_{SYSCLK}=3 MHz		0.49		mA
		CLK_SYS_DIV=2, F_{SYSCLK}=1.5 MHz		0.41		mA
Sleep mode (deep sleep)	I_{SDN}	Call sys_shutdown function, then LFOSC module is disabled		300		nA
Sleep mode (RTC)	I_{RTC}	Call sys_shutdown function, then the internal LFOSC module is enabled and the internal LPOSC (32 kHz) is selected.		800		nA
OTP code loading [2]	I_{LOAD}			4.6		mA

Notes:

[1]. The program runs the While(1) loop, and the GPIO has no load.

[2]. *Charge Pump* is enabled. See CUS_SYSCTL20 register description for details.

1.15 AC Specifications

Table 15. AC Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level output	V_{OH}	Load is 1 kΩ, VDD = 3.3 V	VDD-0.4			V
Low level output	V_{OL}	Load is 1kΩ, VDD = 3.3 V			0.4	V
High level input	VIH	VDD = 3.3 V		0.7*VDD		V
		VDD = 2.0 V		0.7*VDD		V
Low level input	V_{IL}	VDD = 3.3 V		0.2*VDD		V
		VDD = 2.0 V		0.2*VDD		V
Port leakage current	I_{LKG}	VDD = 2.0 V – 3.6 V		TBD		nA

1.16 Typical Performance of High-frequency Transmission

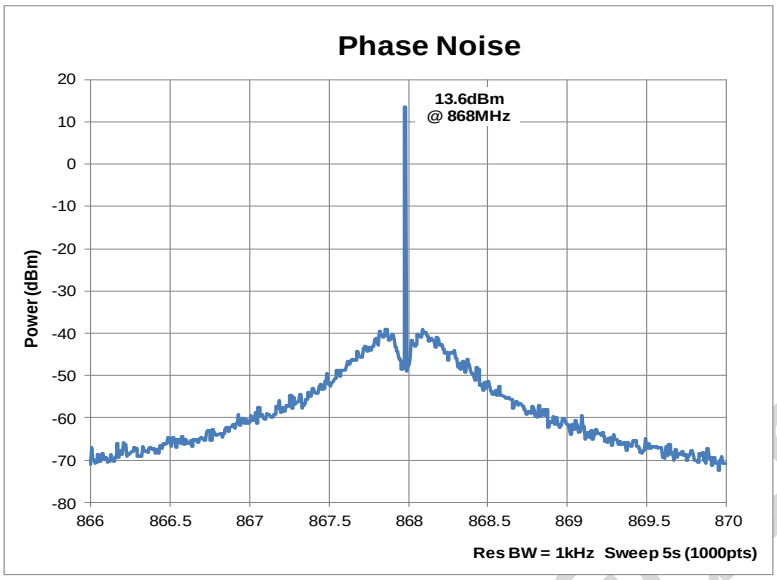


Figure 1. Phase Noise @ F_{RF} = 868 MHz, P_{OUT} = +13 dBm, un-modulated

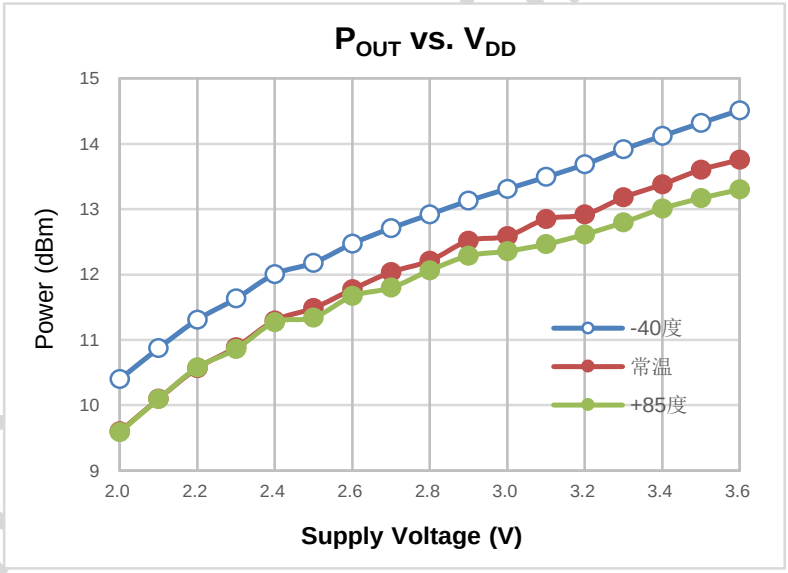


Figure 2. Output Power Vs. Supply Voltage

F_{RF} = 433.92 MHz, P_{OUT} = +13 dBm

2 Pin Description

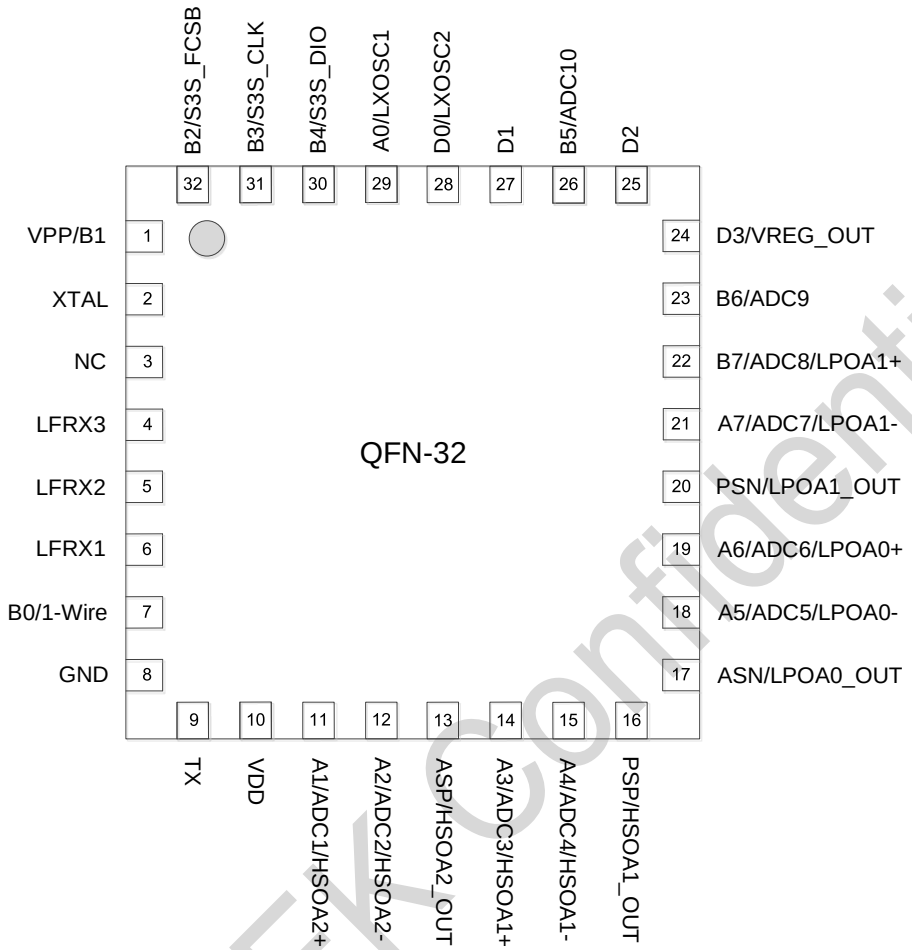


Figure 3. CMT2168A QFN32 Pin Arrangement

Table 16. CMT2168A Pin Description

Pin#	Name	Type		Description
1	VPP/B1	IO	B1	GPIO9, one of the general purpose GPIOs
		A	VPP	OTP programming VPP, 6.5 V voltage input pin
2	XTAL	A		Crystal input pin, connect 26 MHz crystal to GND. See *Section 1.4 Oscillator Specifications* for details.
3	NC			Floating. Don't connect
4	LFRX3	A		Low-frequency wake-up Z-axis antenna input pin
5	LFRX2	A		Low-frequency wake-up Y-axis antenna input pin
6	LFRX1	A		Low-frequency wake-up X-axis antenna input pin
7	B0/1-Wire	IO	B0	GPIO8, one of the general purpose GPIOs
		IO	1-Wire	1-wire chip debugging line
8	GND	A		Power ground
9	TX	A		Single-ended PA RF output pin

Pin#	Name	Type		Description
10	VDD	A		Power supply input pin
11	A1/ADC1/HSOA2+	IO	A1	GPIO1, one of the general purpose GPIOs
		A	ADC1	ADC1, ADC sampling channel 1
		A	HSOA2+	High-speed operational amplifier 2 positive input
12	A2/ADC2/HSOA2-	IO	A2	GPIO2, one of the general purpose GPIOs
		A	ADC2	ADC2, ADC sampling channel 2
		A	HSOA2-	High-speed operational amplifier 2 negative input
13	ASP/HSOA2_OUT	A	ASP	No function
		A	HSOA2_OUT	High speed operational amplifier 2 output
14	A3/ADC3/HSOA1+	IO	A3	GPIO3, one of the general purpose GPIOs
		A	ADC3	ADC3, ADC sampling channel 3
		A	HSOA1+	High-speed operational amplifier 1 positive input
15	A4/ADC4/HSOA1-	IO	A4	GPIO4, one of the general purpose GPIOs
		A	ADC4	ADC4, ADC sampling channel 4
		A	HSOA1-	High-speed operational amplifier 1 negative input
16	PSP/HSOA1_OUT	A	PSP	No function
		A	HSOA1_OUT	High-speed operational amplifier 1 output
17	ASN/LPOA0_OUT	A	ASN	ADC11, ADC sampling channel 11
		A	LPOA0_OUT	Micro-power operational amplifier 0 output
18	A5/ADC5/LPOA0-	IO	A5	GPIO5, one of the general purpose GPIOs
		A	ADC5	ADC5, ADC sampling channel 5
		A	LPOA0-	Micro-power operational amplifier 0 negative input
19	A6/ADC6/LPOA0+	IO	A6	GPIO6, one of the general purpose GPIOs
		A	ADC6	ADC6, ADC sampling channel 6
		A	LPOA0+	Micro-power operational amplifier 0 Positive Input
20	PSN/LPOA1_OUT	A	PSN	ADC12, ADC sampling channel 12
		A	LPOA1_OUT	Micro-power operational amplifier 1 output
21	A7/ADC7/LPOA1-	IO	A7	GPIO7, one of the general purpose GPIOs
		A	ADC7	ADC7, ADC sampling channel 7
		A	LPOA1-	Micropower operational amplifier 1 negative input
22	B7/ADC8/LPOA1+	IO	B7	GPIO15, one of the general purpose GPIOs
		A	ADC8	ADC8, ADC sampling channel 8
		A	LPOA1+	Micro-power operational amplifier 1 positive input
23	B6/ADC9	IO	B6	GPIO14, one of the general purpose GPIOs
		A	ADC9	ADC9, ADC sampling channel 9
24	D3/VREG_OUT	A	VREG_OUT	Internal regulator 2.2 V output, supporting up to 0.5 mA load
		A	D3	Constant current source D3 output driver port
25	D2	A		Constant current source D2 output driver port
26	B5/ADC10	IO	B5	GPIO13, one of the general purpose GPIOs
		A	ADC10	ADC10, ADC sampling channel 10
27	D1	IO		GPIO16, one of the general purpose GPIOs

Pin#	Name	Type		Description
28	D0/LXOSC2	--	D0	No function
		A	LXOSC2	External 32.768 kHz crystal
29	A0/LXOSC1	IO	A0	GPIO0, one of the general purpose GPIOs
		A	LXOSC1	External 32.768 kHz crystal
30	B4/S3S_DIO	IO	B4	GPIO12, one of the general purpose GPIOs
		IO	S3S_DIO	Chip burning bus S3S, burning data line
31	B3/S3S_CLK	IO	B3	GPIO11, one of the general purpose GPIOs
		IO	S3S_CLK	Chip burning bus S3S, burning clock line
32	B2/S3S_FCSB	IO	B2	GPIO10, one of the general purpose GPIOs
		IO	S3S_FCSB	Chip programming bus S3S, programming chip selection line

3 Functional Description

Embedded with a Sub-1 GHz OOK / (G)FSK transmitter, the CMT2168A is a high-performance 8051 SoC, suitable for low-power wireless transmission applications in the 27 - 960 MHz band. The series chips integrate the below major modules [1].

- High-performance 8051 core with rich peripheral resources.
- Sub-1G OOK / (G) FSK transmission module.
- 3D low-frequency receiving/wake-up module (LFRX).
- Powerful analog front end module (AFE).

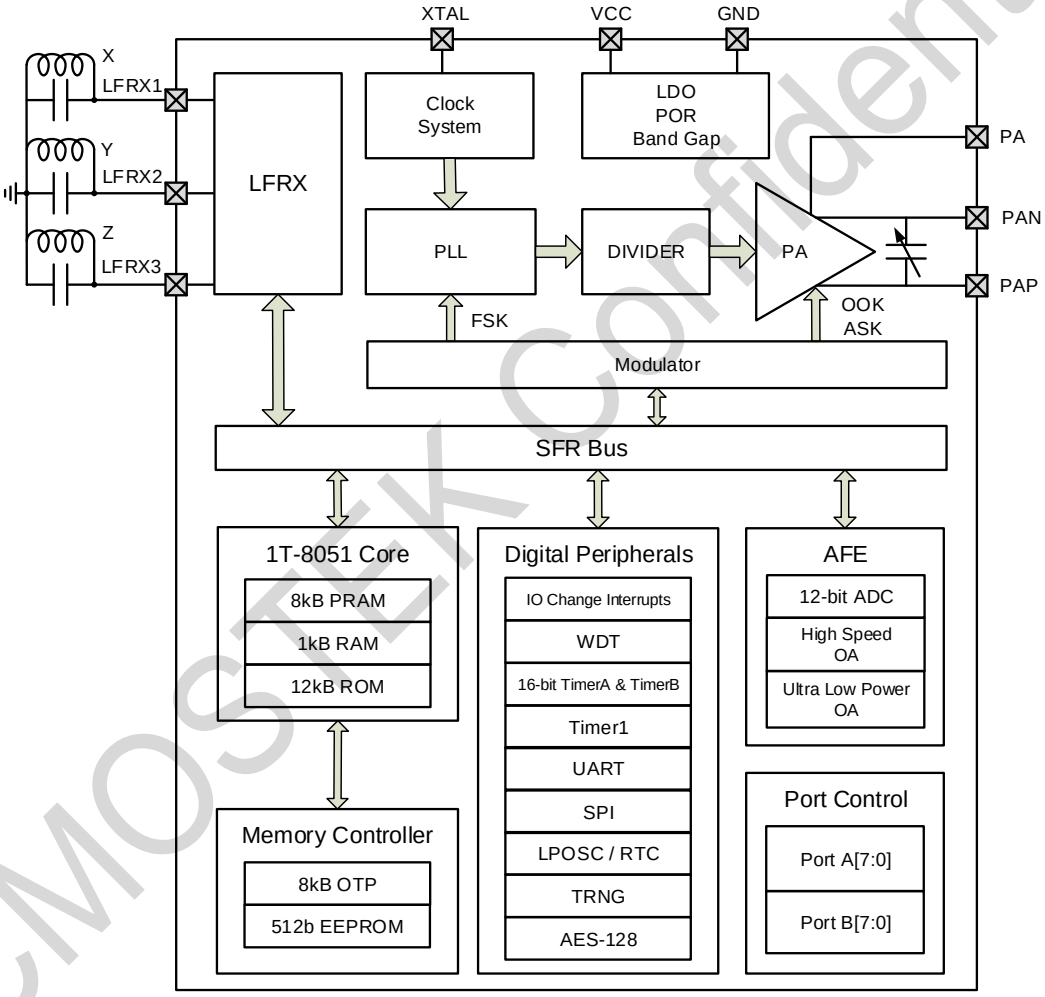


Figure 4. System Block Diagram

Notes:

1. This is the general block diagram for CMT216xA series. Different product models consist of different module combinations, namely not all models provide the full function modules.

3.1 High-performance 8051

Built-in with enhanced 1T-8051 and 24 MHz high-speed RC oscillator, the CMT2168A supports dual-clock operating mode. achieving 24 MIPS high-speed operating. Meanwhile, the low-speed clock is provided by the internal low-speed 32 kHz RC oscillator or external 32.768 kHz crystal oscillator , serving as the clock source of the low-power RTC.

For memory architecture, the on-chip 8 kB OTP ROM is for code storage, 8 kB PRAM for code running, 1 kB XRAM for data storage and 512 bits EEPROM for key data storage in case of power loss. Meanwhile, it integrates 12 kB MASK ROM for the storage of API library function of various chip modules.

For digital peripherals, it supports on-chip AES-128 operation acceleration engine, true random number generator, one UART, one SPI, watchdog, two 16-bit multi-function timers, one RTC, and 16 ports with multiplexing functions.

For development and debugging, the CMT216xA series chips adopt 1-wire debugging interface, which requires only one single wire connecting to the debugger to download code to PRAM, achieving simple and convenient online debugging.

3.2 Sub-1G Transmission Module

The CMT2168A integrates a high-performance Sub-1G transmitter, which applies a high-efficient single-ended Class E PA architecture, achieving p to +13 dBm transmission power while consuming only a current of 18 mA.

The transmitter supports 3 modulation modes, OOK, GFSK and FSK. Appling the fractional phase-locked loop technology, it requires only one 26 MHz crystal oscillator to achieve most of the 27～960 MHz band coverage.

3.3 3D Low-frequency Receiving/waking-up Module

Integrating a 3D low-frequency receiving/waking-up module, the CMT2168A supports operating in listening mode with a low power consumption of 4.6 μA, reaching a wake-up sensitivity of 70 uVrms. It supports digital RSSI with a dynamic range of 80 dB. This product model is a suitable for various active RFID based near-field identification application scenarios.

3.4 High-performance Analog Front End (AFE)

The high-performance AFE module mainly consists of 3 sub-modules including 12-bit high-precision successive approximation analog-to-digital converter (SAR-ADC) with up to 12 channels, 2-channel high-speed and low-power operational amplifier and 2-channel micro-power operational amplifier. It supports various sensor interfaces, which can form instrumentation amplifier with programmable gain or non-inverting amplifier, providing a flexible and suited solution for sensor acquisition application scenarios.

4 Ordering Information

Table 17. CMT2168A Ordering Information

Model	Description	Packaging	Package Option	Operating Condition	Minimum Ordering Quantity
CMT2168A-EQR[1]	27 - 960 MHz transmitter SoC	QFN32	T&R	2.0 to 3.6 V, - 40 to 85 °C	3000

Notes:

[1]. E refers to extended Industrial product rating, which supports a temperature range from -40 to +85 °C.

Q refers to the packaging type QFN32.

R refers to Tape & Reel package type, and the minimum ordering quantity (MOQ) is 3000 pieces.

Please visit www.cmostek.com for more product/product line information.

Please contact sales@cmostek.comor your local sales representative for sales or pricing requirements.

5 Packaging Information

The packaging information of the CMT2168A is shown in the below figure.

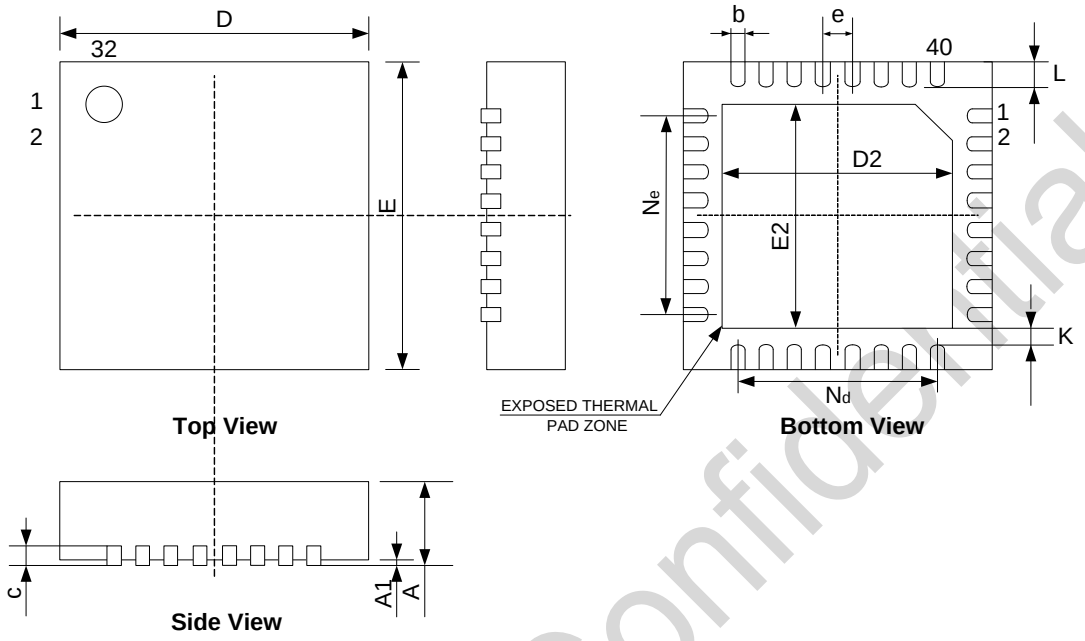


Figure 5. QFN32 Packaging

Table 18. QFN32 5x5 Packaging Scale

Symbol	Scale (mm)		
	Min.	Typ.	Min.
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50 BSC		
Ne	3.50 BSC		
Nd	3.50 BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45

6 Top Marking

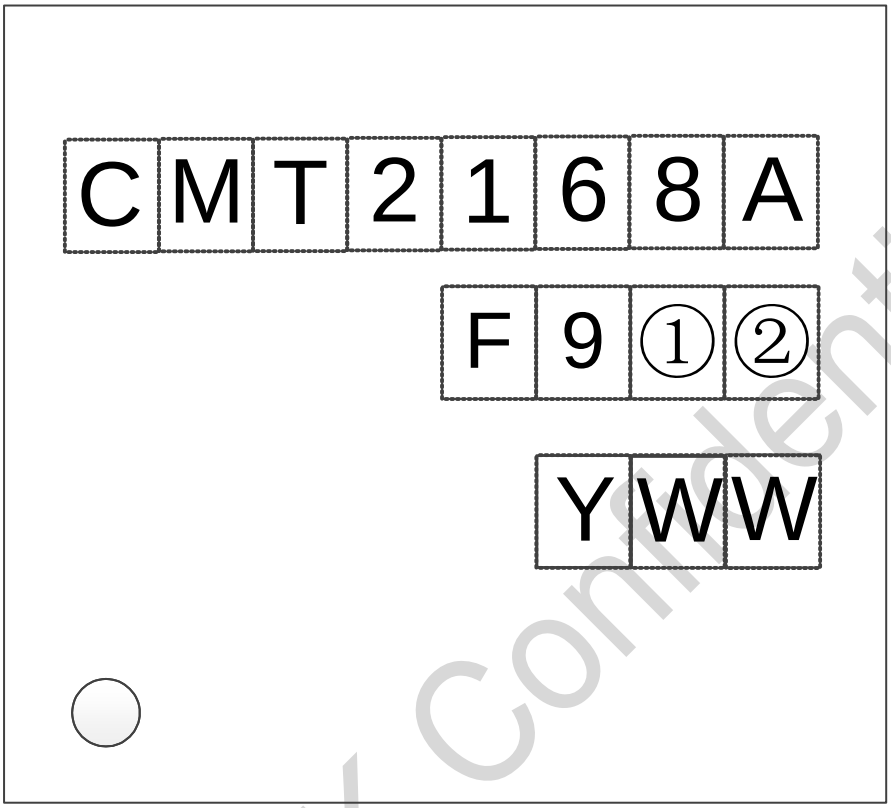


Figure 6. CMT2168A Top Marking

Table 19. CMT2168A Top Marking Information

Marking Method	Laser
Pin 1 Mark	Diameter of the circle = 1 mm
Font Size	0.5 mm, align right
Line 1 Marking	CMT2168A refers to model CMT2168A.
Line 2 Marking	F9 ①② is the internal tracing code.
Line 3 Marking	YWW is the date code assigned by the package factory. Y is the last digit of the year. WW is the working week

7 Related Documents

Table 20. CMT2168A Related Documents

Doc No.	Document Name	Description
AN290	CMT216x User Guide	CMT216xA series chips user guide.
AN280	CMT216xA Low-frequency Receiving Function User Guide	CMT216xA 3D low-frequency receiving function user guide.
AN281	CMT216xA ADC and AFE User Guide	CMT216xA series chip ADC and analog front end user guide.
AN282	CMT216xA API Function Library User Guide	CMT216xA series chip API function library user guide.
AN284	CMT216xA Development Environment Establishment and Debugging	CMT216xA development environment establishment and debugging quick start guide.
AN286	CMT216xA Register Guide	CMT216xA series chip SFR register detail description.

8 Revise History

Table 21. Revise History Records

Version No.	Chapter	Description	Date
0.6	All	Initial version	2019-07-01
0.7	All		2019-11-01

9 Contacts

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